

Real-time finite difference bifurcation diagrams from analog electronic circuits

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Bifurcation diagrams are a convenient way of displaying the variety of behaviors exhibited by nonlinear systems. One of the simplest nonlinear systems is a finite difference equation with a quadratic return map. This system exhibits a range of behaviors: stability, periodic oscillations, and chaos. We present simple inexpensive electronic circuits that perform analog computations of bifurcation diagrams for finite difference equations with quadratic return maps. These bifurcation diagrams, including one for the logistic equation, are easily displayed on an oscilloscope and agree well with analytical and computational predictions. © 2004 American Association of Physics Teachers. [DOI: 10.1119/1.1643374]

I. INTRODUCTION

Valuable experience can be gained in understanding nonlinear systems by constructing a physical nonlinear system, and then comparing collected data to theoretical predictions. In 1985 Mishina, Kohmoto, and Hashi¹ described a simple analog electronic circuit of a finite difference equation with a quadratic return map. They showed that interesting dynamic behavior is easily seen on an oscilloscope. In this paper we modify their circuit so that the bifurcation diagram can be easily displayed, even on an inexpensive 20-MHz analog oscilloscope. It is worth emphasizing to students that the analog circuit, unlike a digital circuit, is a nonlinear physical system.

The finite difference equation investigated in Ref. 1 is

$$x_{i+1} = f(x_i) = 1 - ax_i^2. \quad (1)$$

If the parameter a is between 0 and 2, and if $-1 < x_i < +1$, then x_{i+1} will also be between -1 and $+1$, and the resulting iterated values of x exhibit a variety of behaviors, some of which are shown in Fig. 1. The asymptotic behavior (after the transient response has died out) includes stability, periodic oscillations, and chaos.

A bifurcation diagram is a convenient way of displaying the behavior of a system.²⁻⁴ Figure 2 is the bifurcation diagram computed numerically from Eq. (1). A bifurcation diagram is a visual summary of the values of x that are visited during the asymptotic behavior for each value of a . The bifurcation points are the values of a where the system changes its behavior, for example, from period 1 behavior as in Fig. 1(a) to period 2 oscillations as in Fig. 1(b). The creation of this bifurcation diagram, with its complex behavior arising from the simple mapping of an ordinary parabolic function, is likely to be a rewarding aesthetic experience for both students and instructors.

Another parabolic return map is the logistic equation, a well-known finite difference equation used to model population evolution:⁵

$$x_{i+1} = f(x_i) = Rx_i(1 - x_i). \quad (2)$$

If the parameter R is between 0 and 4 and if $0 < x_i < 1$, then $0 < x_{i+1} < 1$. Because of the popularity of Eq. (2) as an introduction to nonlinear systems, we also present the experimental bifurcation diagram from a circuit constructed to perform an analog computation of Eq. (2).

This project combines an introduction to nonlinear dynamics and electric circuit design. It does not require familiarity with differential equations. There are many examples of electric circuits that are analog computers of nonlinear differential equations and that exhibit a variety of behaviors.⁶⁻⁹ An in-depth treatment of finite difference equations may be found elsewhere.²⁻⁴

II. DESCRIPTION OF CIRCUITS

Figure 3 shows the circuit schematic for producing the bifurcation diagram of Eq. (1). The analog computation uses the same approach as Ref. 1 with the use of an analog multiplier and sample-and-hold ICs. We use the Analog Devices AD633 multiplier because the AD533 is obsolete. The circuit linearly increases the parameter a in Eq. (1). This increase allows the display of the bifurcation diagram on an oscilloscope. The circuit uses ± 15 - and $+5$ -V power supplies. Most of the electrical components are easily available. The AD633 is available from Newark Electronics. General-purpose op amps may be used (LF411, for example).

Acceptable inputs to the AD633 multiplier IC are -10 to $+10$ V. The output voltage is the product of the inputs divided by 10 V. So x_i in Eq. (1) is represented by the voltage V_i , where $x_i = V_i/10$. (The numerical value of V_i is given by the number of volts.) V_i at both inputs of the first AD633 (U1) produces $V_i^2/10$ at the output. The second AD633 (U2) multiplies $V_i^2/10$ by a voltage in the range of 0–2 V representing the parameter a . The output $aV_i^2/100$ is then subtracted from 1 V by the first op amp (U4) circuit. Multiplication by 10 at the second op amp (U5) circuit gives the result V_{i+1} and x_{i+1} in Eq. (1). The LF398 sample-and-hold ICs (U6 and U7) hold this value for use in the next iteration of Eq. (1). A 555 timer (U8) is used to control the sampling times of the LF398 ICs. It is set so that an iteration takes 20 μ s.

The 1-V reference is provided by a regulator arrangement of NPN transistors Q3 and Q4, resulting in a stable reference that is nearly immune to power supply variations. (A 10% variation in the $+5$ -V supply results in about a 1% change in the 1-V reference.) Alternatively 1 V can be obtained from a voltage divider. If so, it must be adjusted while connected to the subtraction op amp (U4) circuit to compensate for the input impedance.

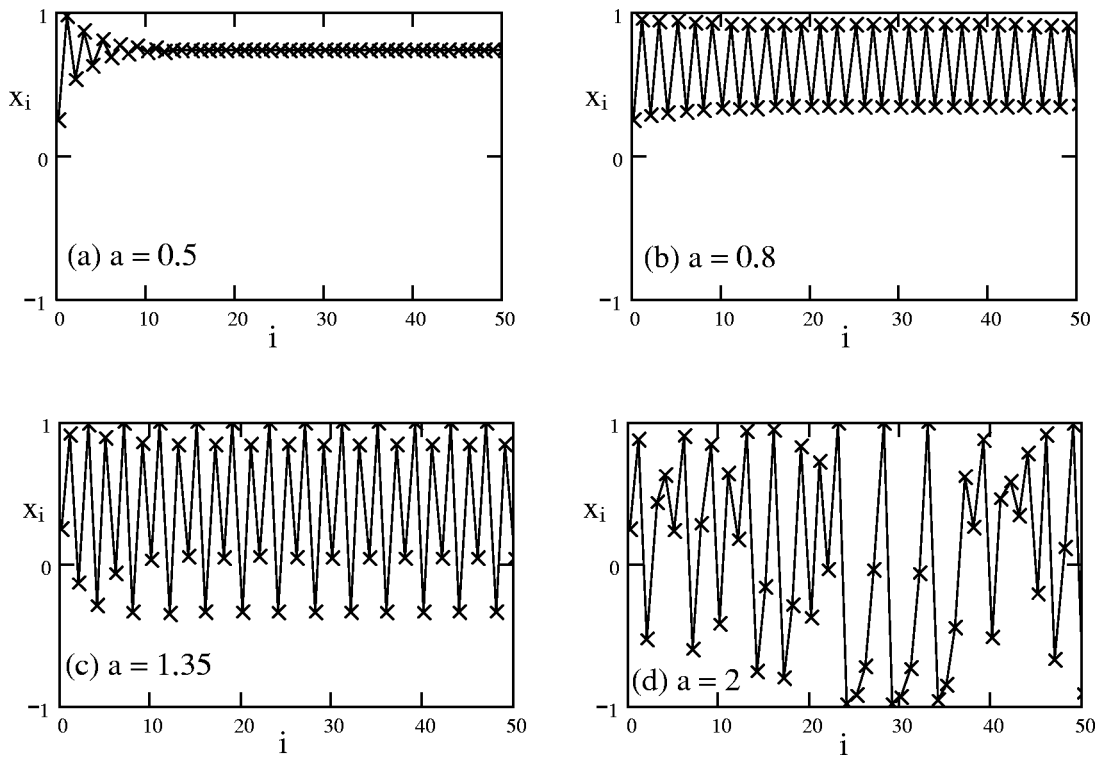


Fig. 1. Dynamic behavior of Eq. (1) for different values of parameter a . (a) $a=0.5$ (stable); (b) $a=0.8$ (period 2); (c) $a=1.35$ (period 4); (d) $a=2$ (chaos). The values are indicated by (\times); the connecting lines are for clarity only. The initial value in all cases is $x_0=0.25$. Note that the transient response has died out by $i=15$.

The voltage ramp circuit is designed to ramp the parameter a from 0 to 2 V in 100 ms. A 555 timer (U3) based circuit controls the ramp. The negative edge of the output of the 555 also provides a convenient trigger for display on an oscilloscope. The 20- μ s iteration period and the 100-ms ramp time result in 5000 iterations of Eq. (1) for each sweep of the parameter a . A triangle or saw tooth wave from a signal generator can be used as an alternative to the 555 based voltage ramp. However, one should be aware that the dc level of many signal generators tends to drift, thus changing the initial and final voltages of the ramp.

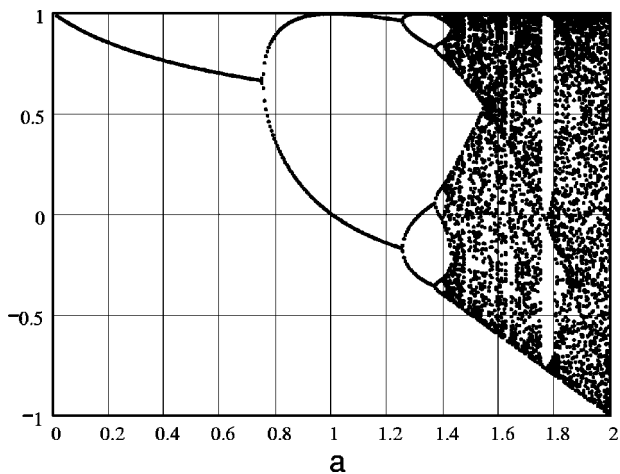


Fig. 2. Bifurcation diagram corresponding to Eq. (1). The visited values of x (after the transient response) are plotted vs the parameter a . Bifurcation from stable to period 2 oscillation occurs at $a=0.75$.

The resistors R1, R8, and R10 are all shown with nominal values. These values need to be adjusted to precisely set the 1-V reference and the voltage ramp. R10 sets the duration of the ramp, and R1 sets the slope of the ramp. Ramp durations of 20, 50, and 100 ms (corresponding to settings of 2, 5, and 10 ms per division on standard oscilloscopes) work well for the oscilloscope display. The values shown in Fig. 3 ramp the parameter a by 2 V in 100 ms. For a 50-ms ramp duration, the nominal values for R1 and R10 are 50 and 80 k Ω , and for 20 ms they are 20 and 32 k Ω .

Figure 4 shows the circuit used to perform the analog computation of the logistic map, Eq. (2). The parameter R is ramped linearly from 0 to 4 V in 100 ms. Note that a small voltage (≈ 15 mV) is added to the Z input of the second AD633. Equation (2) has one fixed point [where the parabola intersects the line $f(x)=x$] when $0 < R < 1$ and two fixed points when $1 < R < 4$. As R increases from zero, the value of x remains at the fixed point $x=0$. When R increases past 1, the fixed point at $x=0$ becomes unstable, and the second fixed point appears at $x=1-1/R$. To ensure that x moves in the positive direction away from the unstable point at $x=0$, a small positive voltage is added as noted. Otherwise, when $x=0$ becomes unstable, the system may move in the negative direction to the negative supply limit.

Problem 1. Confirm that the circuit in Fig. 4 performs the calculation in Eq. (2). [Note that a 10-V reference is used because the 1 in Eq. (2) is put into the circuit prior to the AD633s and thus before division by 10.]

Problem 2. Why is it not necessary to add a small voltage to the Z input in Fig. 3 for calculation of Eq. (1)? (Consider the behavior of the fixed point as a increases from 0.)

The circuit in Fig. 4 uses only half the output range of the

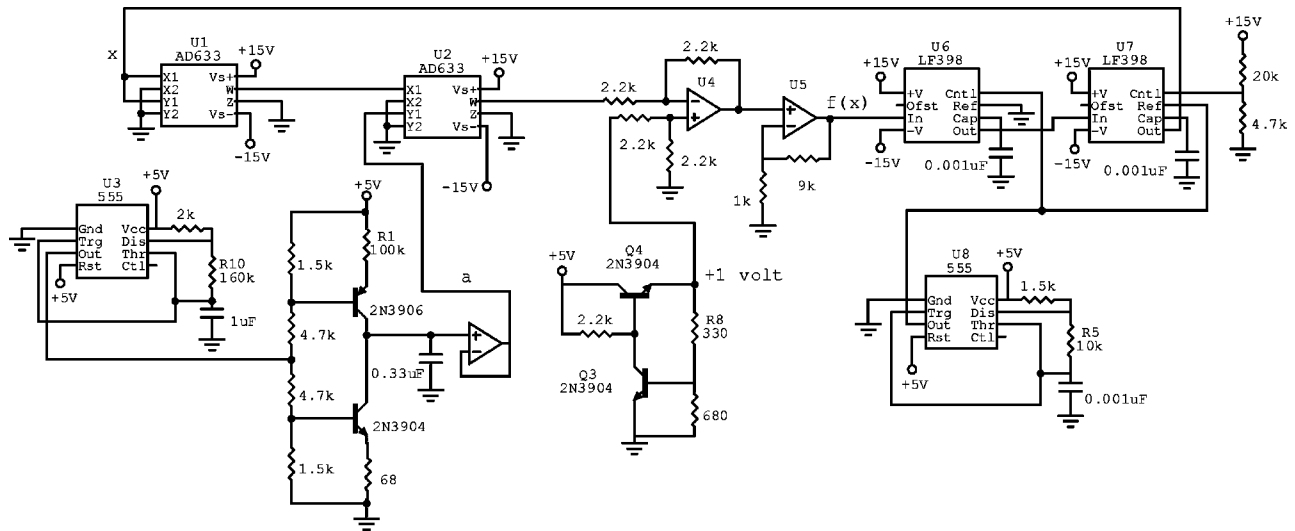


Fig. 3. Schematic for analog computation of the bifurcation diagram of Eq. (1). The voltages corresponding to x , $f(x)$, a , and the 1-V reference are indicated.

AD633 in its calculation of the bifurcation diagram of the logistic equation. The full range of -10 to $+10$ V can be used by modifying the circuit in Fig. 3 to calculate the return map

$$f(x) = a - 1 - ax^2. \quad (3)$$

Equation (3) is equivalent to the logistic equation's return map Eq. (2). This equivalence can be shown by shifting both x and $f(x)$ by 1 and scaling by $1/2$. The new variable is $y = (x + 1)/2$ and the new function $(f(x) + 1)/2$ in terms of y is

$$\begin{aligned} \frac{1}{2}[f(2y-1)+1] &= \frac{1}{2}[a-1-a(2y-1)^2+1] \\ &= 2ay(1-y) = Ry(1-y), \end{aligned} \quad (4)$$

where $R = 2a$. Thus the range -1 to $+1$ for x corresponds to 0 to $+1$ for y , and the range 0 to 2 for a corresponds to 0 to 4 for R .

Equation (3) uses the same range of a as Eq. (1), so it is convenient to include a switch in the circuit to choose which

bifurcation diagram is calculated. As was the case for the circuit in Fig. 4, a small voltage at the Z input of the second AD633 moves x in the positive direction from the fixed point at $x = -1$ when x becomes unstable. In this case a small negative voltage (≈ -15 mV) does the job. This small voltage can be obtained as in Fig. 4 except that the voltage divider connects to the -15 -V supply instead of the $+15$.

Problem 3. Modify the circuit in Fig. 3 to calculate $a - 1 - ax^2$. (Note that the voltages a and 1 are already available for use in an op amp subtraction circuit.)

III. RESULTS

Figure 5 shows the bifurcation diagram as seen on an inexpensive 20-MHz analog oscilloscope. The time scale is 10 ms/div and the vertical scale is adjusted for -10 to $+10$ V full scale. Triggering is from the negative slope of the output of the 555 IC in the voltage ramp circuit; 5000 iterations of

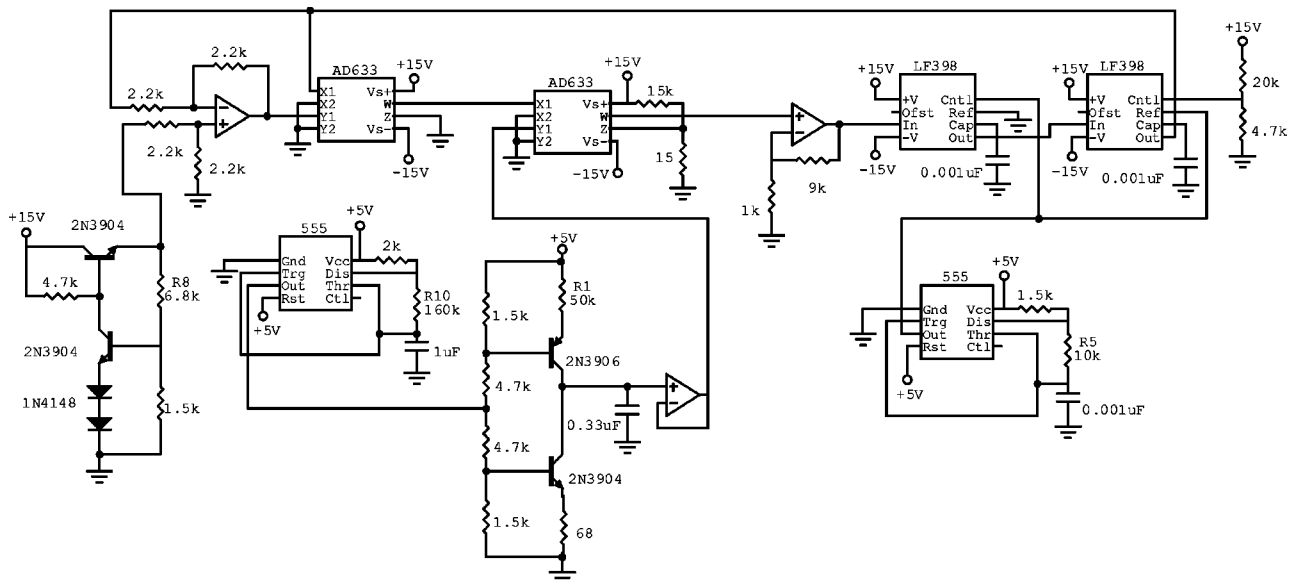


Fig. 4. Schematic for the analog computation of the bifurcation diagram of Eq. (2).

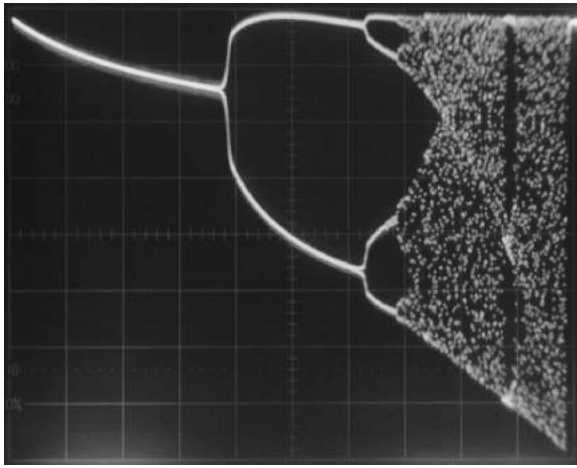


Fig. 5. Oscilloscope trace of output from analog circuit computation of the bifurcation diagram of Eq. (1). The full screen sweep is 100 ms corresponding to parameter a in Eq. (1) going linearly from 0 to 2. The vertical scale is adjusted for -10 to $+10$ V.

Eq. (1) are displayed in a single trace. The parameter a increases to 2 V in 100 ms or 0.2 V per division. The vertical scale is 2.5 V per division or 0.25 units of x per division, because one unit in x corresponds to 10 V. Note how well the data in Fig. 5 resemble the computed bifurcation diagram in Fig. 2. Bifurcations to period 2 and period 4 oscillations, and the region of period 3 oscillations are clearly visible. The noise in Fig. 5 is due to the output transient of the LF398 sample-and-hold IC.

Figure 5 shows that x is stable and decreases from 1 to $2/3$ as a increases from 0 to 0.75. A bifurcation occurs at $a = 0.75$ as the system goes from stable to period 2 oscillations. At $a = 1$ (the midpoint of the horizontal axis), the two x values are 0 and 1.

Figure 6 shows the bifurcation diagram displayed on the oscilloscope measured from the circuit constructed to compute the logistic equation, Eq. (2). The parameter R increases to 4 V in 100 ms or 0.4 V per division. The vertical scale is adjusted for a full scale of 0 to 10 V, or 0.125 units of x per division. Figure 6 agrees well with the bifurcation diagram for the logistic equation.²⁻⁴

The modification of the circuit in Fig. 3 to calculate the logistic bifurcation diagram using Eq. (3) gives a result very similar to Fig. 6. However the vertical full scale is adjusted for the AD633's full range of -10 to $+10$ V.

Of course a digital storage oscilloscope may also be used. If so, it is best to select dot display instead of vector display. The persistence and averaging may be adjusted for optimal appearance.

IV. CONCLUSION

This electronic circuit project provides a good introduction to nonlinear systems. The circuit is based on a simple non-

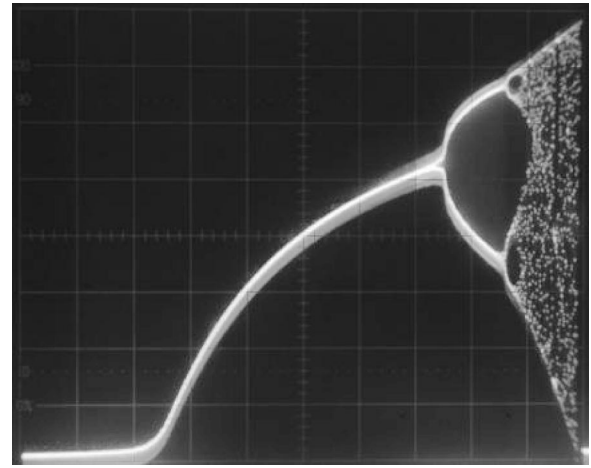


Fig. 6. Oscilloscope trace of the output from analog circuit computation of the bifurcation diagram of Eq. (2). The full screen sweep is 100 ms corresponding to the parameter R in Eq. (2) increasing linearly from 0 to 4. The vertical scale is adjusted for 0 to $+10$ V.

linear system, a finite difference equation with a quadratic return map. The experimental data are in the form of bifurcation diagrams which are easily displayed on an inexpensive analog oscilloscope and agree with predictions. This project should be considered complimentary to the procedures described in Ref. 1. The time evolution and the return maps (x_{i+1} vs x_i) shown in Ref. 1 are valuable projects in addition to the ones described here. They also investigate coupled nonlinear systems.

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¹T. Mishina, T. Kohmoto, and T. Hashi, "Simple electronic circuit for the demonstration of chaotic phenomena," *Am. J. Phys.* **53**, 332-334 (1985).

²G. L. Baker and J. P. Gollub, *Chaotic Dynamics* (Cambridge U.P., Cambridge, 1996), 2nd ed.

³R. C. Hilborn, *Chaos and Nonlinear Dynamics* (Oxford U.P., New York, 1994).

⁴D. Kaplan and L. Glass, *Understanding Nonlinear Dynamics* (Springer-Verlag, New York, 1995).

⁵R. M. May, "Simple mathematical models with very complicated dynamical behavior," *Nature* (London) **261**, 459-467 (1976).

⁶T. P. Weldon, "An inductorless double scroll chaotic circuit," *Am. J. Phys.* **58**, 936-941 (1990).

⁷T. L. Carol, "A simple circuit for demonstrating regular and synchronized chaos," *Am. J. Phys.* **63**, 377-379 (1995).

⁸J. C. Sprott, "Simple chaotic systems and circuits," *Am. J. Phys.* **68**, 758-763 (2000).

⁹B. K. Jones and G. Trefan, "The Duffing oscillator: A precise electronic analog chaos demonstrator for the undergraduate laboratory," *Am. J. Phys.* **69**, 464-469 (2001).