
Question 1

Consider the non-pipelined, 5-stage CPU architecture of [HP]. Assume the following control signals are used in the CPU:

PC Load
IR Load
NPC Load
register A Load
register B Load
register Imm Load
ALUoutput Load
LMD Load
MA select
MB select
MD select
Register write (RW)
Memory Read (MR)
Memory write (MW)
Function select (FS) (5-bit)

Consider the execution of

ADD R1, R2, R3
LD R4, -16(R5)

Make a table showing the values of the control signals for each of the 10 clock pulses for the non-pipelined execution of the above instructions. Use x to denote “don’t care”. Assume function select for ADD operation is 01001.

10% of the assignment mark is for typesetting. Figures and special symbols can be drawn/written by hand.