
Question 1

Solve problem 14.1 on Page 643 of [MK] but use the following sequence of memory (read) addresses (in hexadecimal):
54, 64, 58, F0, 104, 54, 5C, 108, 60, F0, 64, 54, 58, 10C, 5C, 110, 60, F0, 64.

Show all your work. For example, you should indicate, for each memory address, whether it is a cache hit or miss. If it is a hit, at which cache slot the required data is found, and, if a miss, at which cache slot the data will be stored. Further, if the cache slot is overwritten, you should also indicate the memory address of the overwritten data.

Use the following format for your answer (the first memory reference is shown). Or, if you prefer, use 3 separate tables (one for each mapping technique).

<table>
<thead>
<tr>
<th>hex</th>
<th>binary</th>
<th>(a) direct</th>
<th>(b) fully associative</th>
<th>(c) 2-way set associative</th>
</tr>
</thead>
<tbody>
<tr>
<td>54</td>
<td>0001010100</td>
<td>miss, load 101</td>
<td>miss, load 000</td>
<td>miss, load 01/a</td>
</tr>
</tbody>
</table>

Notation:
(1) For set associative, use a, b, ... to distinguish between the sets. For example, 00/a and 00/b represent the two cache slots at index 00 for 2-way set associative mapping.
(2) [xyz] represents the data at memory address xyz. In the table, when a cache slot is overwritten, the memory address of the replaced data should also be shown.

Question 2

Solve problem 14.4 on Page 644 of [MK], but assume a two-way set associative mapping is used (instead of direct mapping). Show all your work.

10% of the assignment mark is for typesetting. Figures and special symbols can be drawn/written by hand.