Students will be divided into teams. Each team consists of a software group and a hardware group. Each team will design (hardware and software of) a computer.

**Phase 1: This part is due on Wed. Feb. 21, 2007**

- This part is carried out by software and hardware groups jointly. The instruction set (assembly language) of the computer will be given. You should design the machine language (binary instruction formats: opcodes, operands, etc...). You will need to assign opcodes in some logical and easily decodable fashion to simplify the hardware design.

  Your phase 1 report should contain names of group members, instruction formats, and opcode and instruction format for each assembly language instruction.

**Phase 2: This part is due on Wed. Mar. 14, 2007.**

- **Software group**: Implement the assembler for this machine. The assembler should take assembly code and produce binary machine code. Your assembler should support symbolic addressing for jumps and branches. But for variables, assume the actual address (e.g. displacement mode) is given in the instruction.

  Your phase 2 report should contain names of group members, user manual, and software description. You should also include a short description of each group members part/contribution to this phase of the project. Also turn in (fully documented) code (on diskette or CD).

- **Hardware group**:

  Design the datapath, and the control unit for the integer operations (including memory, jump and branch operations) for this computer. This will be a non-pipelined CPU, but you may use use a multi-stage architecture to facilitate pipelining later. Your design should include the design of all control signals (multiplexer selects, memory and register write signals, internal register load signals, etc...). Turn in the block diagram of the datapath. Clearly write the boolean expression for each control signal. Also include truth tables for each control signal. **Make sure you give your detailed design to the software group of your team.**

  Your phase 2 report should contain names of group members, the block diagram of the datapath and control unit, and truth tables showing how the control signals are derived from the instruction opcode and other specified bits. Include the boolean expressions (formulas) for control signals. You should also include a short description of each group members part/contribution to this phase of the project.
Phase 3: This part is due on Wed. Apr 11, 2007

- **Software group**: Implement a simulator for the (non-pipelined) CPU designed by your hardware group. The assembler is used to produce machine code for an assembly language program. The simulator accepts machine code output from the assembler. It consists of different modules each defined by the datapath designed by the hardware group. For each clock cycle, show for each stage in the pipeline the control signals generated, the input to the stage, the instruction being executed, and the output of the stage.

  **Turn in the final project report containing reports from previous phases plus phase 3 report (similar to phase 2 report).**

- **Hardware group**: Design the pipelined CPU for the integer operations (including memory, jump and branch operations) for this computer. Your design should include the design of all control signals (multiplexer selects, memory and register write signals, internal register load signals, etc...). **Note that in this case the multiplexer selects should also implement forwarding as required by the pipelined operation. You should also design the logic for stalling as needed.** Turn in the block diagram of the datapath. Clearly write the boolean expression for each control signal. Also include truth tables for each control signal. **The CPU should contain the hardware to implement needed stalls and forwarding.**

  **Turn in the final project report containing reports from previous phases plus phase 3 report that includes block diagram and detailed design (as specified for phase 2 report).**

**Presentations**

In addition to the reports that are submitted at each phase of the project, each student will give a short presentation of his/her work on the project. Software groups should demonstrate their assembler and simulator operations on-line.

**Grading**

The project mark for each student is determined by (1) Overall quality of project (group work), and (2) Individual effort and contribution of each student.